IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 5, and 7 and ADD new claim 8, in accordance with the following:

1. (CURRENTLY AMENDED) An abnormality detection device for detecting an abnormality in a communication bus, the device comprising:

a timer counter ~~measuring~~ to measure a time during which a signal transmitted through said communication bus continues to be a first logical level; and

a comparator ~~comparing~~ to compare the time measured by said timer counter with a threshold value and ~~outputting~~ to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus.

2. (ORIGINAL) The abnormality detection device as claimed in claim 1, wherein said timer counter is initialized at intervals determined according to an event signal supplied thereto.

3. (ORIGINAL) The abnormality detection device as claimed in claim 2, comprising at least two units of said timer counter and said comparator, the timer counter in each of said units being individually initialized at said intervals.

4. (ORIGINAL) The abnormality detection device as claimed in claim 1, further comprising:

a plurality of comparison value registers respectively storing a plurality of threshold values; and

a selector selecting a threshold value from among said plurality of said threshold values according to a selection signal supplied thereto so as to supply said threshold value to said comparator.

5. (CURRENTLY AMENDED) An abnormality detection device for detecting an abnormality in a communication bus, the device comprising:

at least two timer counters each ~~measuring~~ to measure a time during which a signal transmitted through said communication bus continues to be a first logical level;

a register to cumulatively ~~adding~~ add the time measured by at least one of said at least two timer counters, the register being initialized at predetermined intervals; and

a comparator ~~comparing~~ to compare the time cumulatively added by said register with a threshold value and ~~outputting~~ to output an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said register surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus.

6. (ORIGINAL) The abnormality detection device as claimed in claim 5,

wherein said register supplies said cumulative time to at least one of said at least two timer counters, and

said at least one of said at least two timer counters measures the time by using said cumulative time as an initial value.

7. (CURRENTLY AMENDED) A microcomputer connected to a communication bus, the microcomputer comprising:

a timer counter ~~measuring~~ to measure a time during which a signal transmitted through said communication bus continues to be a first logical level; and

a comparator ~~comparing~~ to compare the time measured by said timer counter with a threshold value and ~~outputting~~ to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the microcomputer is independent of a CPU controlling the communication bus.

8. (NEW) An abnormality detection device to detect an abnormality in a communication bus, the device comprising:

at least two timer counters each to measure a time during which a signal transmitted through said communication bus continues to be a first logical level;

a register to cumulatively add the time measured by at least one of said at least two timer counters, the register being initialized at predetermined intervals; and

a comparator to compare the time cumulatively added by said register with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said register surpasses said threshold value,

wherein said register supplies said cumulative time to at least one of said at least two timer counters, and

said at least one of said at least two timer counters measures the time by using said cumulative time as an initial value.

INTRODUCTION:

In accordance with the foregoing, claims 1, 5, and 7 are amended to improve clarity and new claim 8 has been added. New independent claim 8 includes claimed features of original claim 5 and objected claim 6. Claims 1-5 and 7 stand rejected and claim 6 stands objected.

Claims 1-8 are pending and under consideration.

REJECTION UNDER 35 U.S.C. § 102:

In the Office Action, at page 2, claims 1-5 and 7 were rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 5,565,856 to Takaba et al. ("Takaba"). The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

Takaba generally describes a logic determination as a bus abnormality. See FIG. 9 and column 6, lines 5-40. When bus 400 is not in an idle state for more than a prescribed period of time, a bus abnormality is determined to have taken place. However, the cited reference fails to teach or suggest, "a comparator to compare the time measured by said timer counter with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value," as recited in independent claim 1. Rather than indicating an abnormality when the time surpasses a threshold value, if the idle state is not more than a prescribed period, then the abnormality is indicated.

Further, Takaba determines an abnormality when ABSY is LO, when there is incomplete communication, or absence of received data. See columns 7, line 50, to column 8, line 50. However, the cited reference fails to teach or suggest the claimed features of the comparator of independent claim 1.

According to Takaba, a controller 100 has three CPUs 110, 120, and 130 conducting various control operations. See column 3, lines 34-35. In addition, the cited reference provides an abnormality detection and a storage of abnormality information at the controller 100. See column 5, lines 3-11. FIG. 5 is a flowchart illustrating, for example, storing a DIAG code corresponding to a particular abnormality in the SEAM regions 2 and 4, when an abnormality is detected during the abnormality detection. See also FIG. 6.

In contrast, according to an aspect of the present invention, independent claim 1 recites, "the abnormality detection device is independent of a CPU controlling the communication bus." Thus, the abnormality may be detected even during communication. Takaba fails

to teach or suggest, "a comparator to compare the time measured by said timer counter with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus," as recited in independent claim 1.

Independent claim 5 recites, "a comparator to compare the time cumulatively added by said register with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said register surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus." However, Takaba fails to teach or suggest such recitations. Rather, the cited reference limits its description to generally provide that in an absence of received data, processing continues and a variable k is set to nDATA as the message length of the received data to finish this processing. See column 8, lines 42-50.

Further, the arguments presented above supporting the patentability of claim 1 having a similar claimed feature are incorporated herein to support the patentability of independent claim 5. It is the Applicants' position that Takaba fails to teach or suggest all the claimed features of independent claim 5. It is respectfully requested that independent claim 5 and related dependent claim 6 be allowed.

Independent claim 7 recites, "microcomputer connected to a communication bus, the microcomputer comprising: a timer counter to measure a time during which a signal transmitted through said communication bus continues to be a first logical level; and a comparator to compare the time measured by said timer counter with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the microcomputer is independent of a CPU controlling the communication bus." The arguments presented above supporting the patentability of claim 1 are incorporated herein to support the patentability of independent claim 7. It is the Applicants' position that Takaba fails to teach or suggest all the claimed features of independent claim 7. It is respectfully requested that independent claim 7 be allowed.